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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,317	01/15/2004	Vincent S. Chang	2003-0287/24061.627	5370
42717	7590	02/15/2006	EXAMINER	
HAYNES AND BOONE, LLP 901 MAIN STREET, SUITE 3100 DALLAS, TX 75202			DEO, DUY VU NGUYEN	
			ART UNIT	PAPER NUMBER
			1765	
DATE MAILED: 02/15/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/758,317

Applicant(s)

CHANG ET AL.

Examiner

DuyVu n. Deo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 December 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (US 2003/0232491) and Shih et al. (US 6,387,761).

Yamaguchi describes a method for forming MOSFET comprising: forming a gate insulator silicon oxide on the substrate (paragraph [0041]); forming a nitrided gate insulator (paragraphs [0042-0045, 0061-0065]); performing a thermal processing (claimed anneal procedure) (paragraphs [0049-0051]); forming a conductive gate structure on a portion of the nitrided gate insulator (paragraphs [0052,0053]); forming a LLD source/drain regions on the substrate using the gate electrode structure as the mask (claimed forming LLD source/drain regions in the area of the substrate not covered by the conductive gate structure) (paragraph [0053]); forming sidewall insulator spacers on the side of the gate structure (paragraph [0054]); forming a heavily doped source/drain regions in the area not covered by the gate structure and the sidewall spacers (paragraph [0055]). Unlike claimed invention, Yamaguchi doesn't describe the annealing process comprises hydrogen. Shih teaches the annealing process is done in N<sub>2</sub>/H<sub>2</sub> gases (col. 4, line 29-67). It would have been obvious for one skilled in the art to modify Yamaguchi's annealing process by adding H<sub>2</sub> because Shih teaches that annealing in N<sub>2</sub>/H<sub>2</sub> would eliminate defects such as pinholes in silicon nitride and cure defects such as dangling

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bonds at the silicon nitride/polysilicon electrode surface to form a high quality interface between silicon nitride and polysilicon electrode. The annealing T is 700-850 degrees C, with a H<sub>2</sub> concentration including 10 % and the annealing time is 60-180 seconds (col. 4, line 53-67).

Referring to claims 2, 3, 10, 13, and 18, the silicon oxide gate insulator is formed by thermal oxidation at a thickness of 10 angstrom (paragraph [0041]) and nitrided silicon dioxide layer would have an equivalent oxide thickness of about 10 angstrom.

Referring to claims 4, 14 the nitride silicon dioxide layer would have a dielectric constant between 3.9-7.8.

Referring to claims 5, 11 the nitrided gate insulator layer is formed by plasma nitridation procedure at 50-3000 Watts using N<sub>2</sub> and He (paragraph [0064]).

Referring to claims 6, 12, Yamaguchi doesn't describe forming the nitrided gate insulator layer by annealing process at T 600-1100 degrees C in either NH<sub>3</sub>, NO, or N<sub>2</sub>O. Shih teaches that nitrided gate insulator can be formed either by a plasma process or a thermal nitridation (claimed annealing) at T 800-950 degree C in NH<sub>3</sub> (col. 4, line 5-27). At the time of the invention, one skilled in the art, in light of Shih, would find it obvious to use either process to form the nitride gate insulator layer with a reasonable expectation of success.

Unlike claimed invention, applied prior art above doesn't describe the anneal procedure is performed in the same tool to be used for deposition of the conductive gate material. However, one skilled in the art at the time of the invention would find it obvious to perform different procedures including the annealing and deposition procedure in the same tool because it would eliminate the down time of transferring substrate to different tools that would reduce

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production yield and it also eliminate the contamination of the substrate when moving from one tool to the other.

***Response to Arguments***

3. Applicant's arguments filed 12/5/05 have been fully considered but they are not persuasive.

Referring to applicant's argument that neither Yamaguchi nor Shih doesn't describe forming a polysilicon gate structure on the hydrogen annealed nitrided silicon dioxide layer, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant's argument that modification of the Yamaguchi reference destroys the purpose or function of the invention disclosed in the reference by adding H<sub>2</sub> into Yamaguchi's process since Yamaguchi's plasma nitridation process already cures the defects is found unpersuasive. Yamaguchi's plasma nitridation is done for a different purpose than Shih's H<sub>2</sub>/N<sub>2</sub> annealing step. Yamaguchi teaches that the plasma nitridation helps the leakage current of the gate insulator made of the silicon oxide film 18 and the silicon nitride film 19 to be reduced thereby enabling a further reduction of the silicon oxide-equivalent thickness of the gate insulator (paragraph [0048]). Shih teaches that annealing in N<sub>2</sub>/H<sub>2</sub> would eliminate defects such as pinholes in silicon nitride and cure defects such as dangling bonds at the silicon nitride/polysilicon electrode surface to form a high quality interface between silicon nitride and polysilicon electrode (col. 4, line 53-67). Even if Shih's annealing step helps to cure defects that

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is reduced by Yamaguchi's plasma nitridation step, doing it again in a different way does not destroy any purpose or function of Yamaguchi's plasma nitridation step but it only helps to further ensure the complete removal of all of the defects and this is would be desired and obvious to one skilled in the art.

Applicant's argument that none of the applied prior art "recognized the problem of decreased etching selectivity for a gate insulator layer comprising of nitrided silicon dioxide" and so "a solution to the problem being obvious only after recognizing of the problem by the applicant" is found unpersuasive because the teaching or the reason for combining of the applied prior art has nothing to do with applicant's recognizing of the problem of decreasing etching selectivity. The reason to modify Yamaguchi in light of Shih is to cure defects such as dangling bonds at the silicon nitride/polysilicon electrode surface to form a high quality interface between silicon nitride and polysilicon electrode (col. 4, line 53-67).

### ***Conclusion***

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DuyVu n. Deo whose telephone number is 571-272-1462. The examiner can normally be reached on 6:00-2:30 Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Primary Examiner

Duy-Vu N. Deo

2/9/06

